UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,208	03/26/2004	Yuen Fai Wong	019959-004200US	8639

20350 7590 02/05/2010

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
PATEL, CHANDRAHAS B	

ART UNIT	PAPER NUMBER
2464	

MAIL DATE	DELIVERY MODE
02/05/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,208	WONG ET AL.	
	Examiner	Art Unit	
	Chandrahas Patel	2464	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,32-47 and 71-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-19 and 32-45* is/are allowed.

6)☒ Claim(s) *20-22,24-30,46,47,71-75,77-80 and 82-84* is/are rejected.

7)☒ Claim(s) *23,71,76 and 81* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/15/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 16-22, filed 11/24/2009, with respect to claims 1-30 and 32-45 have been fully considered and are persuasive. The rejection of 8/24/2009 has been withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 78 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 78 recites the limitation "sending to the second processor" in lines 2-3 of claim 78. Claim 78 depends from claim 75. Neither claim 75 nor claim 78 have a processor in the system that is being claimed. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 20-22, 24-30, 47, 72-74, 80, 82-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956) and Rajkumar et al. (USPN 7,391,769).

Regarding claim 20, Maher, III teaches a circuit for aggregating a plurality of input data streams [**Fig. 2, 100**], the circuit comprising: a first data link adapted to receive the input

data stream via a first data link having a first bandwidth, the input data stream comprising ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet comprising at least one priority factor coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; the aggregation module adapted to analyze and selectively recombine the ingress data packets in response to the at least one priority factor so as to generate an aggregated data **[Col. 7, lines 41-52]**; a memory coupled to the aggregation module, the memory adapted to store analyzed data packets **[Fig. 2, 112]**; and a second data link coupled to the aggregation module, the second data link adapted to output the aggregated data stream from the aggregation module **[Fig. 2, 120, 126]**.

However, Maher, III does not teach generating an aggregated data stream for a second data link having a second bandwidth smaller than the first bandwidth; a first data link is coupled to first processor and a second data link is coupled to second processor; the first data link is adapted to receive the input data stream from the first processor via the first data link; and a second data link outputting the data stream to the second processor.

Scholten teaches a first data link is coupled to first processor and a second data link is coupled to second processor **[Fig. 3, 314, 316]**; the first data link is adapted to receive the input data stream from the first processor via the first data link **[Col. 7, lines 47-49, as can be seen in Fig. 3, 310 transmit FIFOs are coupled to ingress data processors 314 to receive data from 314]**; and a second data link outputting the data stream to the second processor **[Fig. 3, 312 outputs data to plurality of egress processors 316]**. Rajkumar teaches a second data link coupled to the aggregation module, second data link having a second bandwidth smaller than the first bandwidth **[Fig. 1A, output is couple to aggregator 104, Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first bandwidth since only portion of the data that is required is aggregated so information that is being output is less than the information coming in thus bringing down the output data rate **[Fig. 2, 202]** and have processors on input and output port so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]**.

Regarding claim 21, Maher, III teaches each of the first processors and the second processor comprise an interface providing logical interconnection between a Media Access Control sub layer (MAC) and a Physical layer (PHY) **[Fig. 2, 102, 120, Abstract]**.

Regarding claim 22, Maher, III teaches memory is an external buffer memory **[Fig. 2, 112]**.

Regarding claim 24, Maher, III teaches packet analyzer includes a data decoder coupled to ingress data port to decode a header of each ingress data packet to extract the at least one priority factor **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claim 25, Maher, III teaches a read buffer is coupled to common read interface **[Fig. 2, 136]**.

Regarding claim 26, Maher, III teaches a data encoder is coupled to read buffer that encodes the data packets into an interface format corresponding to the first interface before sending from the output port **[Col. 8, lines 26-28]**.

Regarding claim 27, Maher, III teaches a write interface coupled to the packet analyzer, adapted to write the analyzed data packets into the memory at the memory location indicated by the corresponding packet descriptor **[Col. 7, lines 34-46]**.

Regarding claim 28, Maher, III teaches a write buffer coupled between first packet analyzer and first write interface **[Fig. 2, 118]**.

Regarding claim 29, 30, Scholten teaches a flow control module is adapted to assert a flow control if an amount of data stored in buffer exceeds a threshold **[Col. 8, lines 7-29]**.

Regarding claim 47, Maher, III teaches a method for aggregating data packets **[Fig. 2, 100]**, the method comprising: receiving an input data stream from the first port via a first data link having a first bandwidth, the input data stream comprising ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet comprising at least one priority factor coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; generating an aggregated data stream by analyzing and selectively recombining the ingress data packets in response to the at least one priority factor, the at least one priority factor comprising an indication of whether the ingress packet contains protocol data or not **[Fig. 2, 140, Col. 6, lines 15-25]**; and outputting the aggregated data stream to a second port via a second data link having a second bandwidth **[Col. 7, lines 47-52]**.

However, Maher, III does not teach generating an aggregated data stream for a second data link having a first bandwidth greater than the second bandwidth and first data port is coupled to first processor and second data port is coupled to second processor.

Scholten teaches first data port is coupled to first processor and second data port is coupled to second processor **[Fig. 3, 314, 316]**. Rajkumar teaches a second data link coupled to the aggregation module, first data link having a first bandwidth greater than the second bandwidth **[Fig. 1A, output is couple to aggregator 104, Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first bandwidth so that users only utilize the bandwidth needed at a particular time **[Col. 1, lines 53-57]** and have processors on first and second port so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]**.

Regarding claims 72 and 82, Maher, III teaches decoding a header of each ingress data packet to extract the at least one priority factor **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claims 73 and 83, Maher, III teaches encoding the aggregated data packets into an interface format before sending to the second processor **[Col. 8, lines 26-28]**.

Regarding claims 74 and 84, Maher, III teaches analyzing the ingress data packets is performed separately for each data stream **[Col. 7, lines 38-40, Fig. 2, 110]**.

Regarding claim 80, Maher, III teaches a system for aggregating data packets **[Abstract]**, the system comprising: a means for receiving an input data stream from a first data link having a first bandwidth, the input data stream comprising ingress data packets, each ingress data packet comprising at least one priority factor coded therein **[Fig. 2, 102, Col. 6, lines 5-14, 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; means for generating an aggregated data stream by analyzing and selectively recombining the ingress data packets in response to the at least one priority factor, the at least one priority factor comprising an indication of whether the ingress packet contains protocol data or not **[Col. 7, lines 41-52]**; and means for outputting the aggregated data stream to a second data link having a second bandwidth **[Fig. 2, 120, 126]**.

However, Maher, III does not teach a first data link is coupled to first processor and second data link is coupled to second processor; wherein the first bandwidth is greater than the second bandwidth.

Scholten teaches first data link is coupled to first processor and second data link is coupled to second processor **[Fig. 3, 314, 316]**. Rajkumar teaches the first bandwidth is greater than the second bandwidth **[Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first bandwidth so that users only utilize the bandwidth needed at a particular time **[Col. 1, lines 53-57]** and have processors on first and second port so that each processor can format data for transmission and reception **[Col. 8, lines 38-50]**.

6. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Scholten (USPN 7,126,956).

Regarding claim 46, Maher, III teaches a method for aggregating a plurality of input data streams **[Fig. 2, 100]**, the method comprising: receiving an input data stream, each input data stream comprising ingress data packets **[Fig. 2, 102, Col. 6, lines 5-14]**, each ingress data packet comprising at least one priority factor coded therein **[Col. 6, lines 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; generating an aggregated data stream by combining the plurality of input data steams into one aggregated data stream in response to the at least one priority factor, the at least one priority factor comprising an indication of whether the ingress packet contains protocol data or not **[Fig. 2,**

140, Col. 6, lines 15-25], classifying each of the ingress data packets into one of a plurality of priority classes based on the at least one priority factor [**Col. 7, lines 34-53, packets are stored in different queues according to their priority**]; and outputting the aggregated data stream [**Fig. 2, 120**].

However, Maher, III does not teach providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor; wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer.

Scholten teaches providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor [**Col. 8, lines 7-37, analyzer is provided for each processor for determining FIFO fill level and for determining whether data can be transmitted on that port or not**]; wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer [**Col. 8, lines 7-37, receives data and analyzes for buffer fullness for transmission purposes**].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have analyzer so that data can be analyzed for transmission purposes and buffer fill level information [**Col 8, lines 7-37**].

7. Claims 75, 77-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher, III et al. (USPN 6,654,373) in view of Rajkumar et al. (USPN 7,391,769).

Regarding claim 75, Maher, III teaches a system comprising: an input interface having a first bandwidth and configured to receive a data stream, wherein the data stream comprises ingress data packets, each ingress data packet comprising at least one priority factor coded therein **[Fig. 2, 102, Col. 6, lines 5-14, 22-25, type or protocol can be a priority factor as discussed in applicant's specification]**; a module coupled to the input and configured to receive the data stream, analyze the data stream and selectively recombine the ingress data packets in response to the at least one priority factor, the at least one priority factor comprising an indication of whether the ingress packet contains protocol data or not **[Col. 7, lines 41-52]**; and an output interface having a second bandwidth having a second bandwidth and configured to output the recombined ingress data packets **[Fig. 2, 120, 126]**.

However, Maher, III does not teach the first bandwidth is greater than the second bandwidth.

Rajkumar teaches the first bandwidth is greater than the second bandwidth **[Col. 4, lines 50-53, output rate is lower than input rate]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a data stream having less bandwidth than first bandwidth since only portion of the data that is required is aggregated so information that is being output is less than the information coming in thus bringing down the output data rate **[Fig. 2, 202]**.

Regarding claim 77, Maher, III teaches decoding a header of each ingress data packet to extract the at least one priority factor **[Fig. 2, 104, Col. 6, lines 15-25]**.

Regarding claim 78, Maher, III teaches an encoder configured to encode the recombined ingress data packets into an interface format before sending to the second processor **[Col. 8, lines 26-28]**.

Regarding claim 79, Maher, III teaches each ingress data packet is analyzed separately **[Col. 7, lines 38-40, Fig. 2, 110]**.

Allowable Subject Matter

8. Claims 1-19, 32-45 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, prior art teaches all limitations of the claim except an aggregation module coupled to the plurality of ingress data ports and configured to receive the plurality of input data streams from the first processors using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor, the aggregation module adapted to analyze and combine the plurality of input data streams into one aggregated data stream in response to the at least one priority factor and to generate a packet descriptor comprising a reference to a memory location of its analyzed data packet; the memory comprising a plurality of priority queues each provided for a corresponding priority class, adapted to store the packet descriptor of each of the analyzed data packets classified to the corresponding priority class, the packet descriptor containing a reference to the memory location of its analyzed data packet in the memory.

This taken with all other limitations of dependent claims is considered novel and non-obvious.

Regarding claim 32, prior art teaches all limitations of the claim except generating a packet descriptor for the analyzed ingress data packet, the packet descriptor containing a

reference to a memory location of its analyzed data packet stored in the memory; placing the packet descriptor in a priority queue corresponding to the priority class of the data packet; arbitrating and selecting a packet descriptor from among the priority queues using selection logic implementing a queue scheme; reading a data packet corresponding to the selected packet descriptor from the memory.

This taken with all other limitations of dependent claims is considered novel and non-obvious.

10. Claims 23, 71, 76 and 81 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chandrahas Patel whose telephone number is (571)270-1211. The examiner can normally be reached on Monday through Thursday 7:30 to 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2464

/Chandrahas Patel/
Examiner, Art Unit 2464